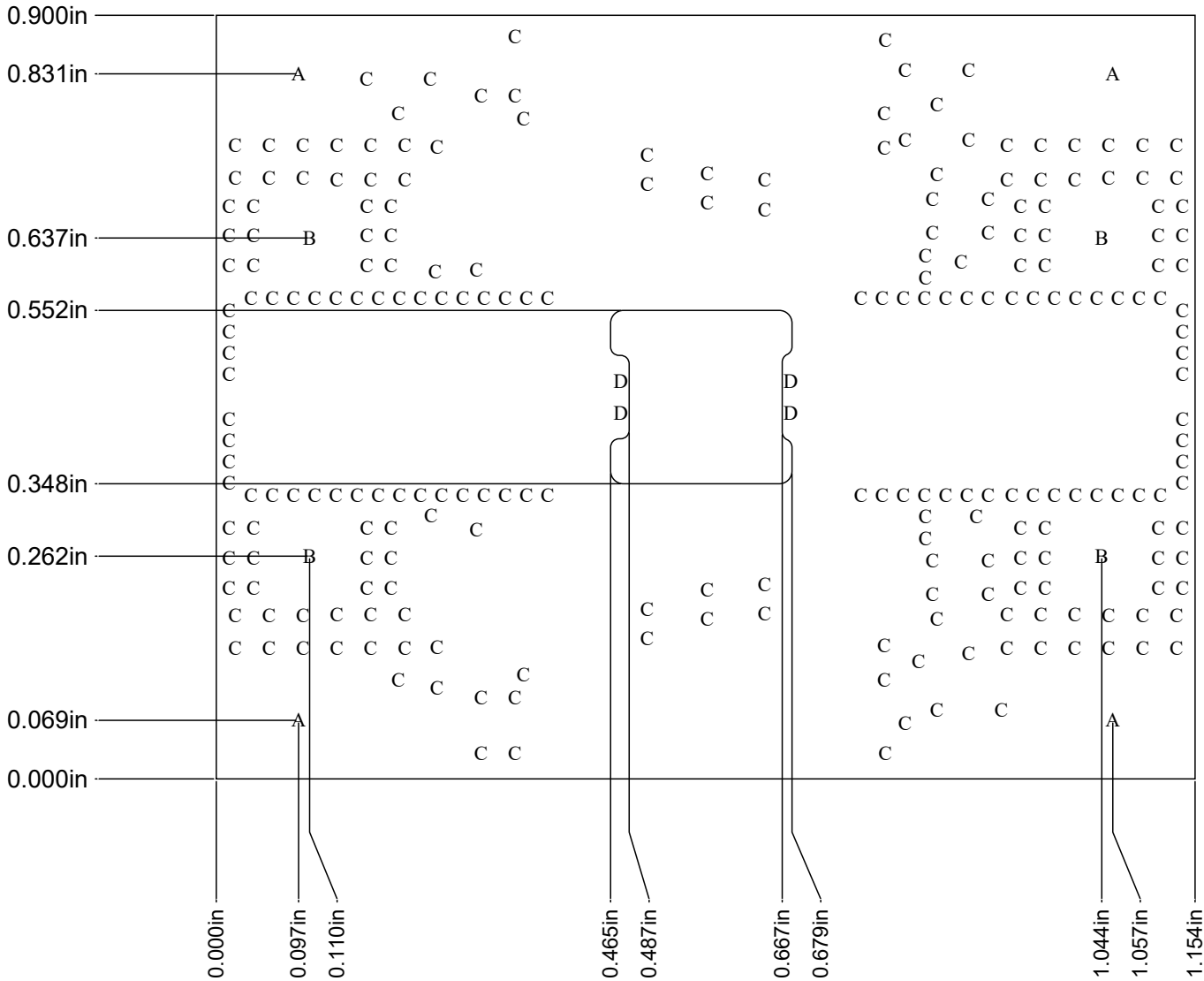


SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD
SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS
COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. NUMBER OF LAYERS: 2 LAYERS
METAL 1 0.5oz. (Plus Plating)
CORE 1: TACONICS TSM-DS3B, .005in. THICK
METAL 2 0.5oz. (Plus Plating)
SOLDERMASK TOP: LPI (LIQUID PHOTO-IMAGEABLE), GREEN OR LDI (LASER DIRECT IMAGEABLE),
GREEN. MAX FINISH THICKNESS OF SOLDERMASK TO BE 0.001in.
SILKSCREEN TOP: HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
4. FINISH PLATING:
A. METAL 1(TOP) AND METAL 4(BOTTOM):
ENEPIG (ELECTROLESS NICKEL, ELECTROLESS PALLADIUM, IMMERSION GOLD)
ENEPIG PLATING POST SOLDERMASK (ONLY ON OPENINGS)
5. FINISHED BOARD THICKNESS: (0.009in) ±.003IN.
6. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP)
AND METAL 2 (BOTTOM) EXCEPT AROUND CONNECTOR AREA.
7. TOLERANCE: PC BOARD OUTLINE:
A. PC BOARD OUTLINE: ±0.002in.TOLERANCE AND IS CRITICAL TO RF PERFORMANCE
B. POSITION OF INTERNAL CUTOUT RELATIVE TO PCB OUTLINE ± .002.
8. METAL TO EDGE IS NECESSARY. THE PRODUCT PERFORMANCE IS SIGNIFICANTLY
COMPROMISED WITH LARGE PULL BACKS. WE WILL ACCEPT BURRS.
9. METALIZATION MUST BE FREE FROM CONTAMINATION AND DEBRIS.
10. BURRS SHALL NOT EXCEED 0.002in.
11. VIA PLATING/FILLING:
ALL PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
12. SINGULATION: EXTERNAL OUTLINE AND INTERNAL CUTOUTS ARE TO BE COMPLETED
VIA OPTICAL (LENZ) ROUTING OR LASER. LASER ROUTING IS AUTHORIZED ONLY IF IT
YIELDS A WIRE-BONDABLE SURFACE ADJACENT TO THE LASER-SAWN EDGE.
13. FINISHED Cu THICKNESS TO BE .0018 ± .0005.
14. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
15. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES
NOT EXIST ON BACKSIDE OF BOARD.
16. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
17. NO VENDOR MARKING ALLOWED EXCEPT DATE CODE FOR TRACEABILITY.
18. BOARDS TO BE SINGULATED PER MECHANICAL 3 AND DELIVERED AS SINGLES
19. NO ELECTRICAL TEST NEEDED.

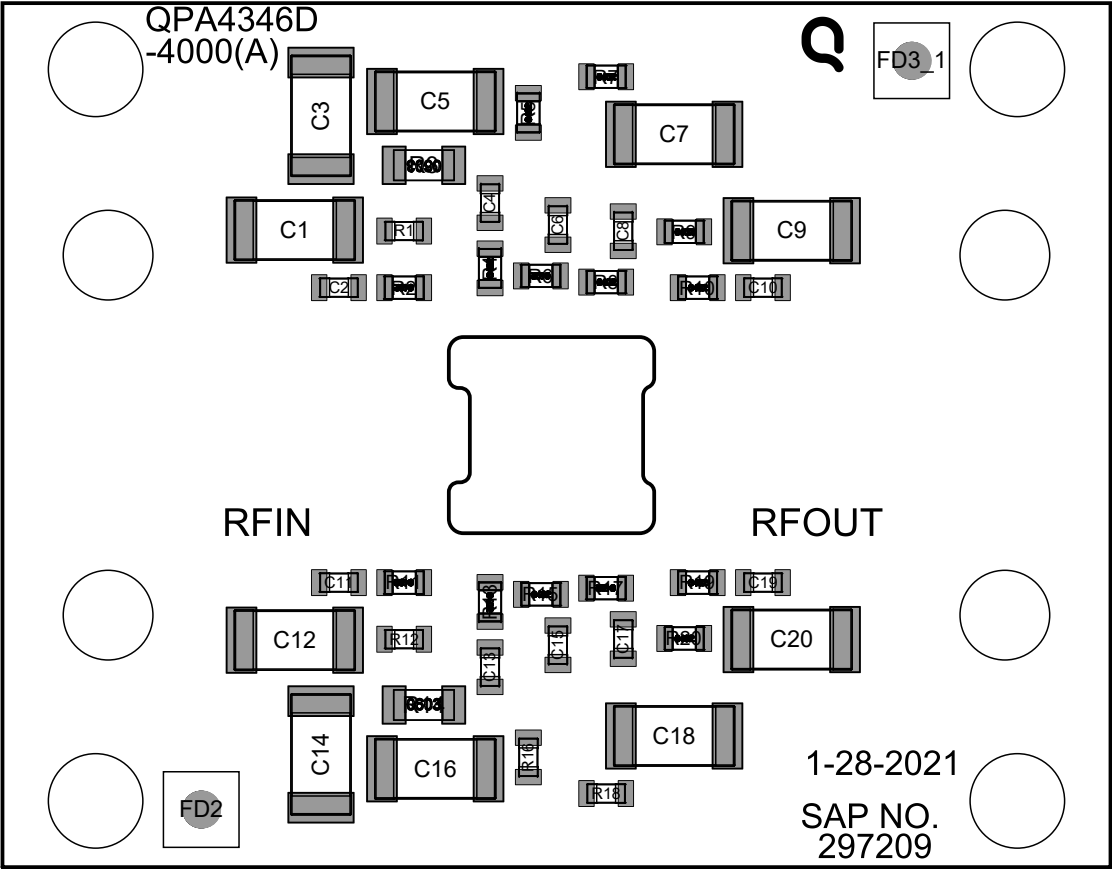
REFERENCE NOTE: Uses QPA4246D-4000[1] CAL SAP No. 297277



* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 297209			
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE			
	DESIGNER	OMARRUFO	DATE	1/28/2021
	ENGR.	M.ROBERG		
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		TITLE: QPA4346D EVALUATION PCB DESIGN PACKAGE	
 THIRD ANGLE PROJECTION DO NOT SCALE DRAWING	SIZE B		DOCUMENT NUMBER: QPA4346D-4000	PROTOTYPE INSTANCE: N/A
	SHEET 1 OF 5		CAD: ALTIUM DESIGNER	REV. A

1. THE PCB WILL MOST LIKELY NOT BE FULLY POPULATED.



LAYER STACK LEGEND_SEE NOTE 3 FOR MATERIAL (COPPER THICKNESS IS @ FINISHED THICKNESS)

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	SILKSCREEN_TOP			Legend	GTO
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask	GTS
Copper	METAL1_TOP	0.0018in		Signal	GTL
Core		0.0050in	TACONICS TSM-DS3B	Dielectric	
Copper	METAL2_BOT	0.0018in		Signal	GBL
Total thickness: 0.0090in					

Drill Table (HOLE SIZES ARE DRILLED SIZE)

Symbol	Count	Hole Size	Plated	Drill Layer Pair
D	4	6.00mil(0.15mm)	Plated	METAL1_TOP - METAL2_BOT
C	236	15.00mil(0.38mm)	Plated	METAL1_TOP - METAL2_BOT
B	4	95.00mil(2.41mm)	Plated	METAL1_TOP - METAL2_BOT
A	4	100.00mil(2.54mm)	Plated	METAL1_TOP - METAL2_BOT
	248 Total			

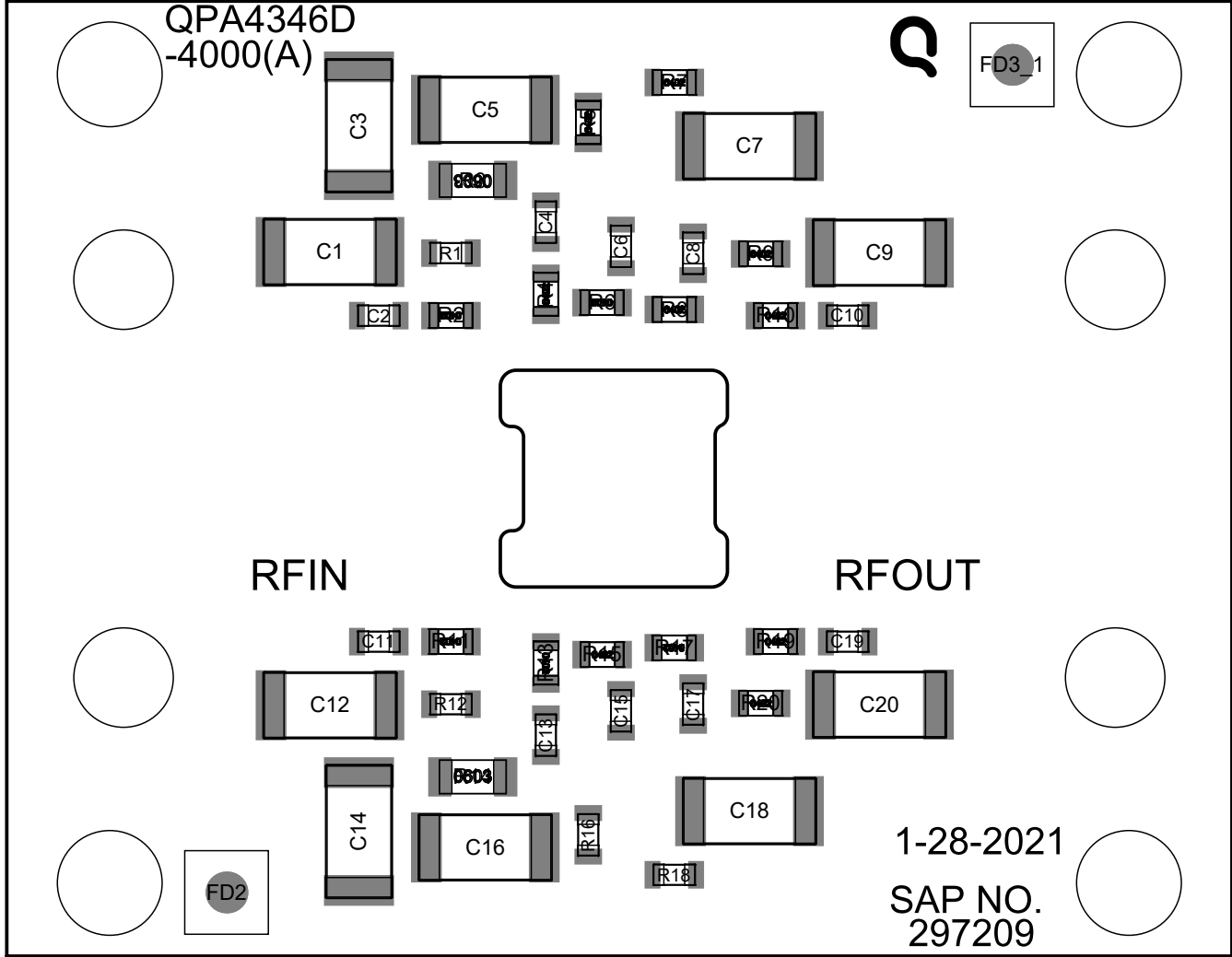
SIZE	DWG. NO.		PROTOTYPE INSTANCE:	REV.
B	QPA4346D-4000		N/A	A
SHEET 2 OF 5	CAD: ALTUM DESIGNER			SCALE: 2:1

Current Date & Time: 3/18/2021 12:56

FOR-001324 REV D

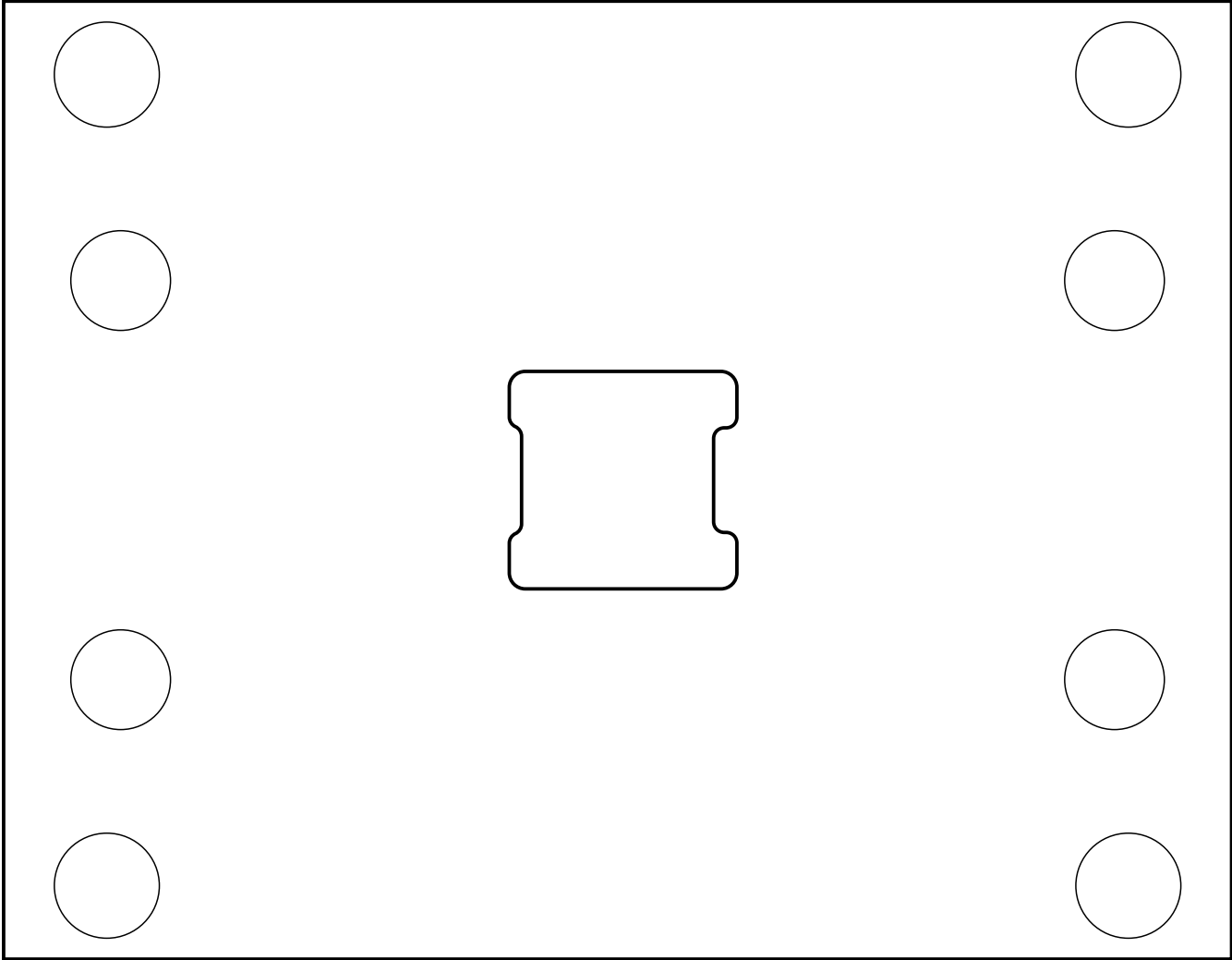
B

TOP ASSEMBLY VIEW



A

BOTTOM ASSEMBLY VIEW

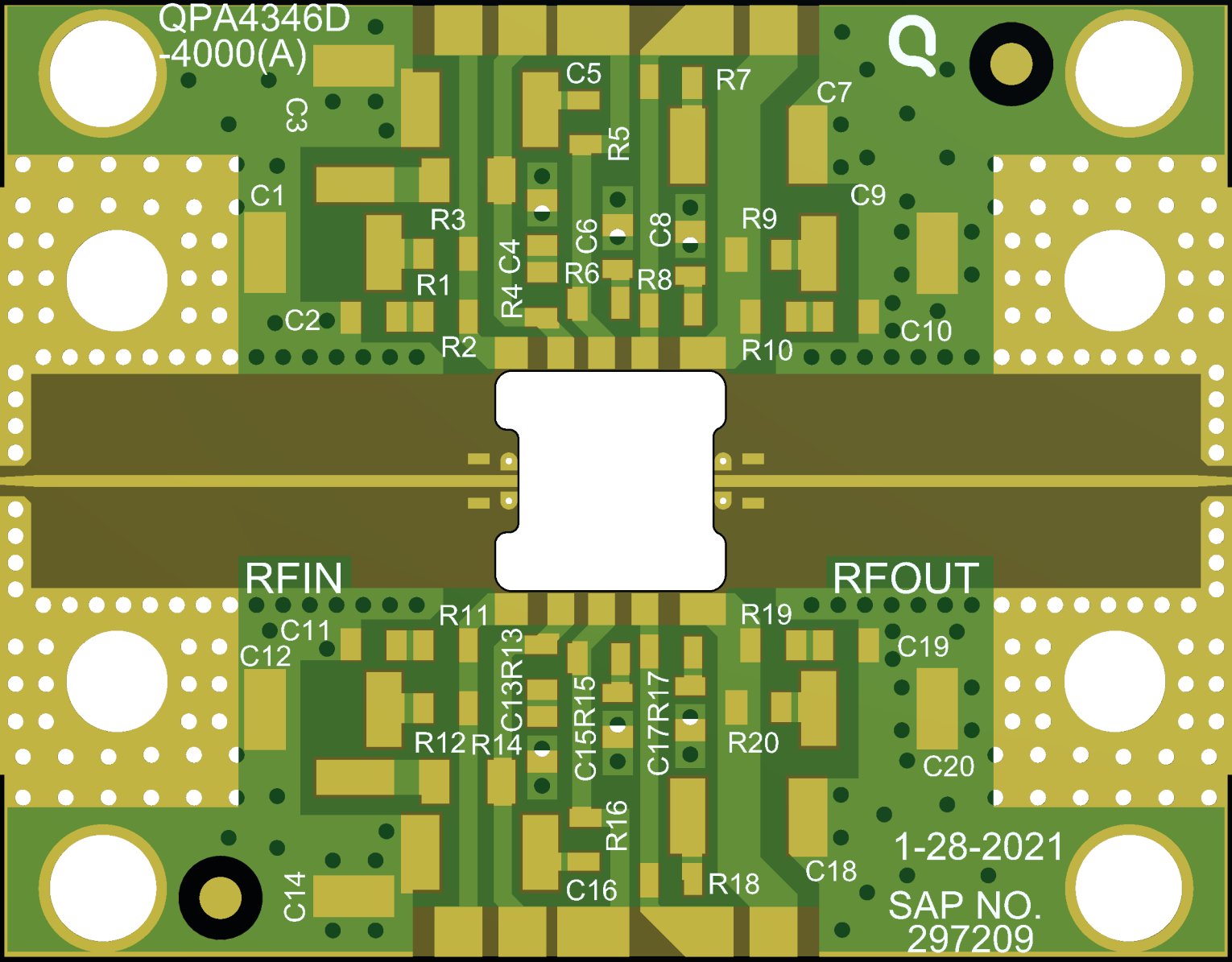


B

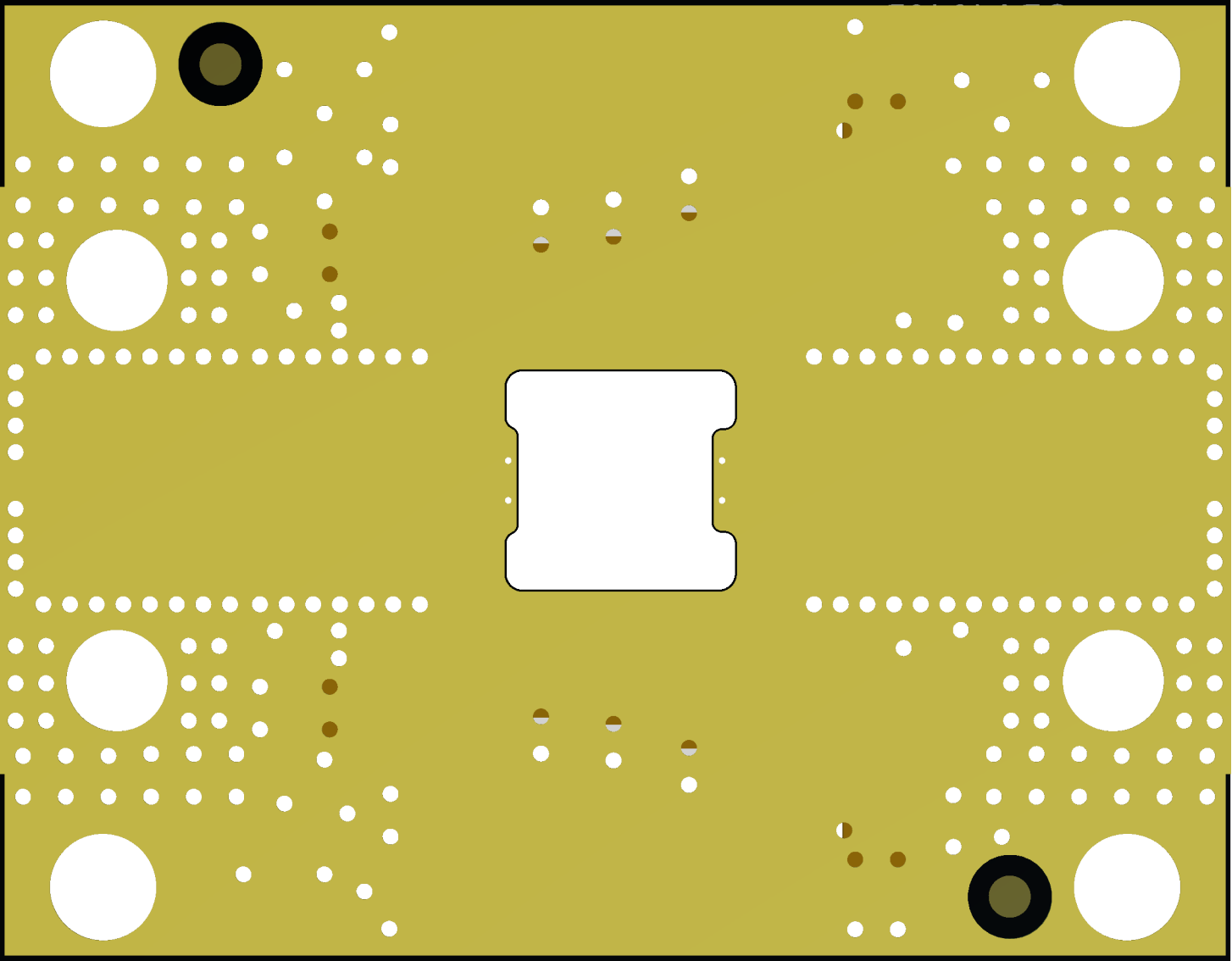
A

SIZE			DWG. NO.	PROTOTYPE INSTANCE:	REV.
B			QPA4346D-4000	N/A	A
SHEET 3 OF 5	CAD: ALTUM DESIGNER			SCALE:	2:1

Top View

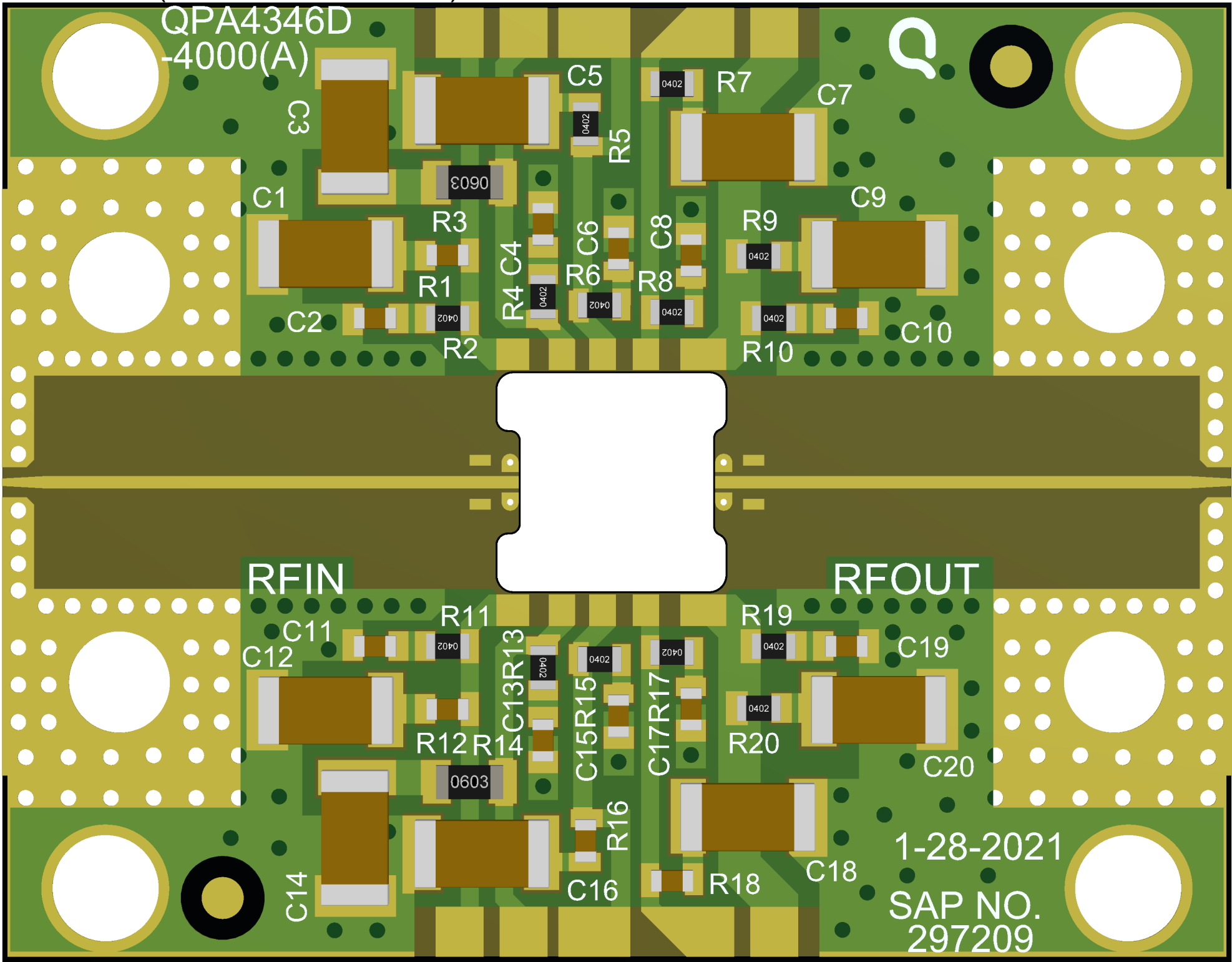


Bottom View



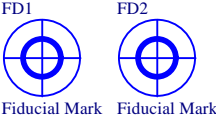
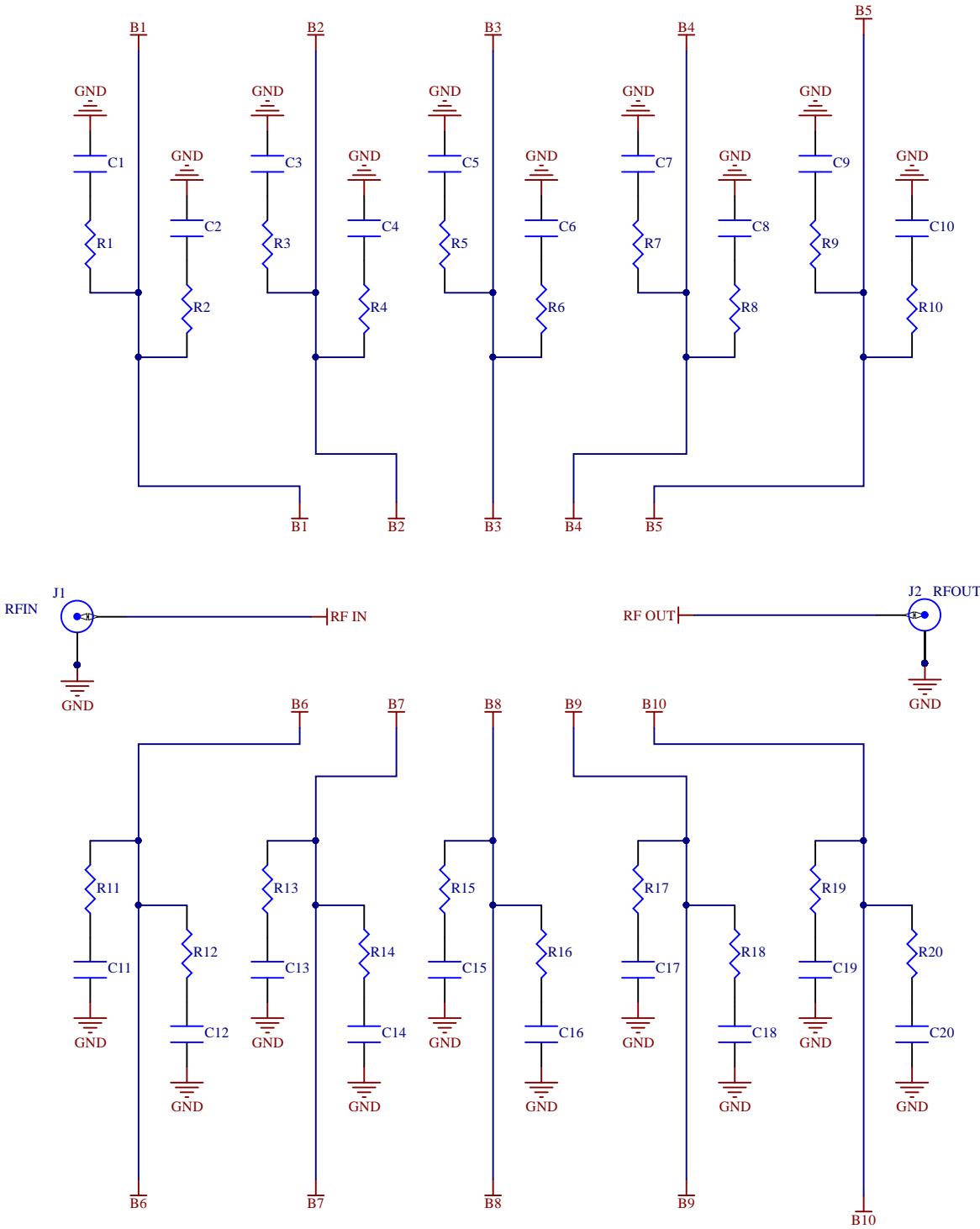
SIZE			DWG. NO.	PROTOTYPE INSTANCE:	REV.
B			QPA4346D-4000	N/A	A
SHEET 4 OF 5		CAD: ALTIUM DESIGNER			SCALE: 2:1

TOP VIEW (FULLY POPULATED)



SIZE	DWG. NO.		PROTOTYPE	REV.
B	QPA4346D-4000		INSTANCE: N/A	A
SHEET 5 OF 5	CAD: ALTIUM DESIGNER		SCALE:	2:1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
A	INITIAL RELEASE	1/28/2021	O.MARRUFO



SAP MATERIAL NUMBER: 297209			
APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE	DATE		
DESIGNER	O.MARRUFO	TITLE: QPA4346D EVALUATION PCB DESIGN PACKAGE	
ENGR.	M.ROBERG		
PDE CONTROLLED		SIZE B	DOCUMENT NUMBER: QPA4346D-4000
		SCALE: NTS	PROTOTYPE INSTANCE: N/A
		REV. A	
		SHEET 1 OF 1	